**Experiment / Assignment / Tutorial No. 5**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| **Batch: B1 Roll No.: 1711072 Experiment / assignment / tutorial No.: 5** |

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| **Title:** Flip Flops |

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**Objective:**Design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

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**Books/ Journals/ Websites referred:**

* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* A.P.Godse, D.A.Godse, “Digital Logic Design”

**Pre Lab/ Prior Concepts:**

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

**JK-flip flop:** has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

**D Flip Flop:** tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

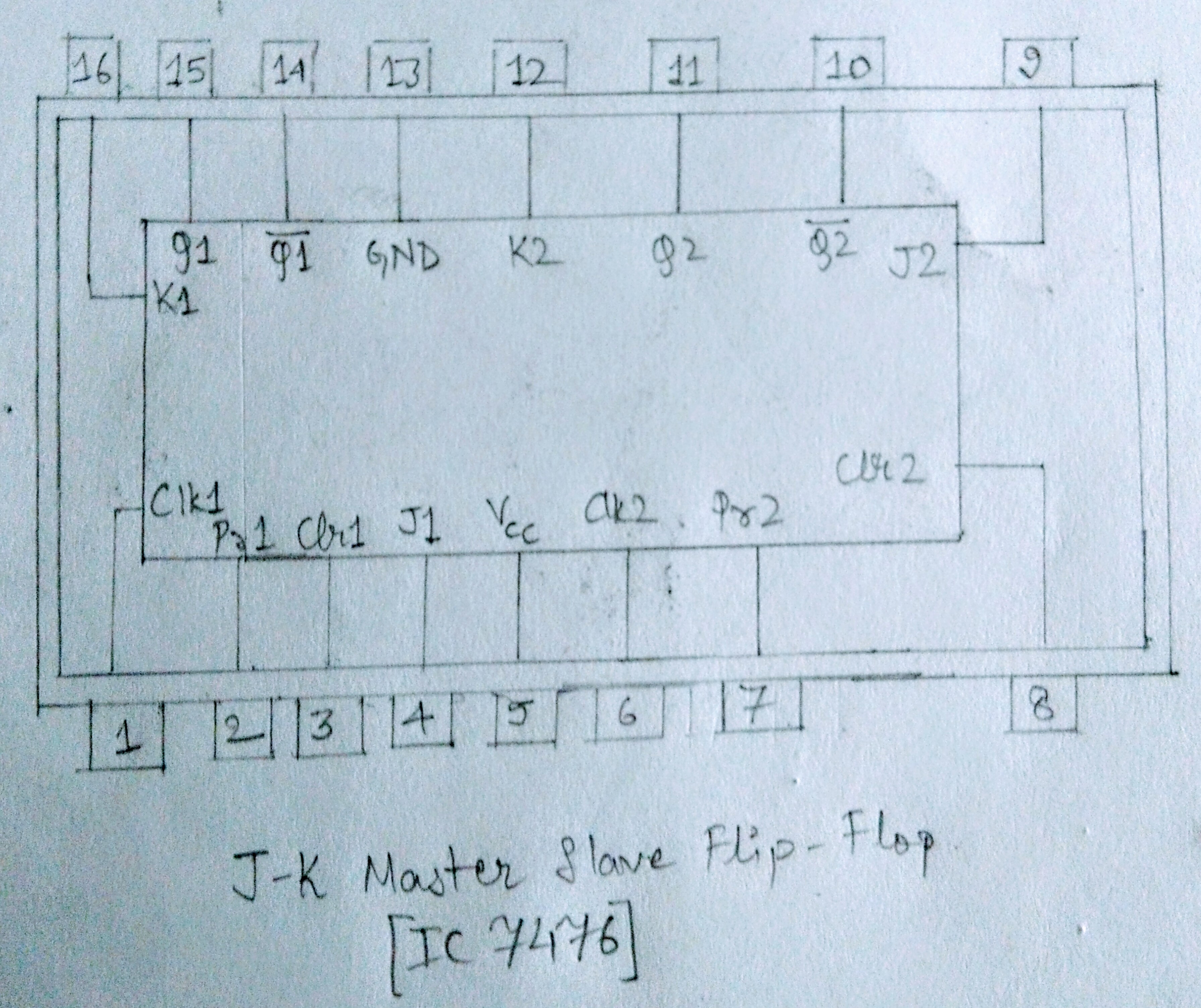
**T Flip Flop:** T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

**Implementation Details:**

**Procedure**

1. Locate IC 7476 on Digital trainer kit
2. Apply various inputs to J & K pins by means of the output on logic output indicator.
3. Connect a pulsar switch to the clock input.
4. Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

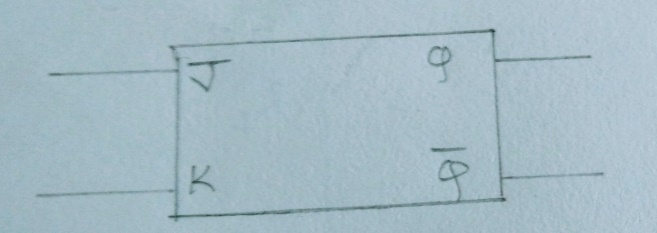
**Pin Diagram of IC 7476 JK Master- Slave FF**



**Logic Symbol**

**JKFF Truth Table**

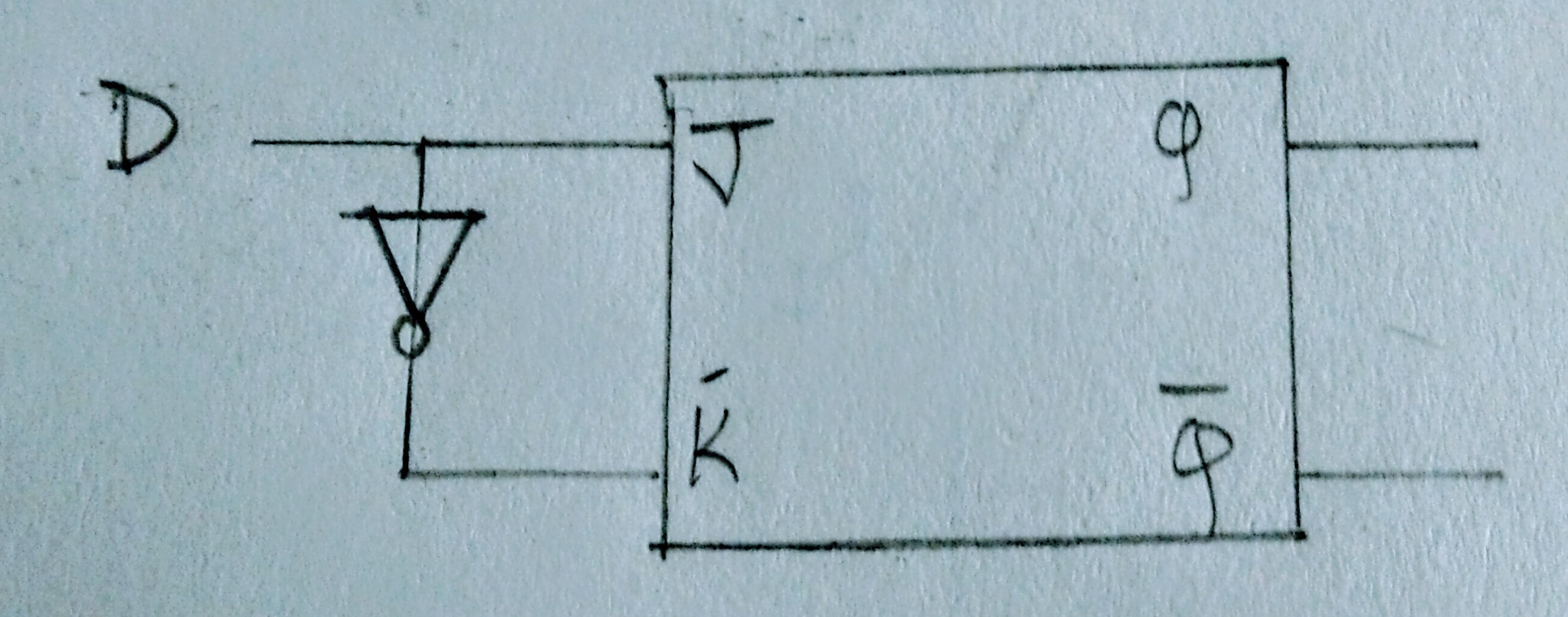
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **J** | **K** | **Q** | **Q’** | **Qn+1** | **Qn+1’**  **n+1** |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |



**D FF Truth Table**

|  |  |
| --- | --- |
| **D** | **O/P** |
| 0 | 1 |
| 1 | 1 |

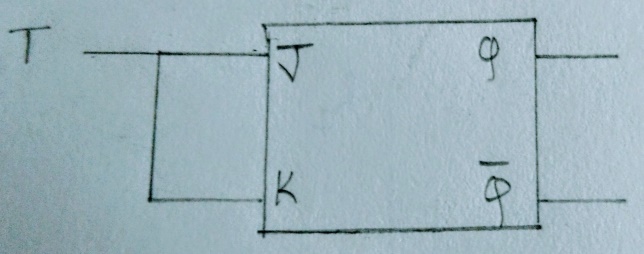
|  |  |  |
| --- | --- | --- |
| **D** | **Qn** | **Qn+1** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



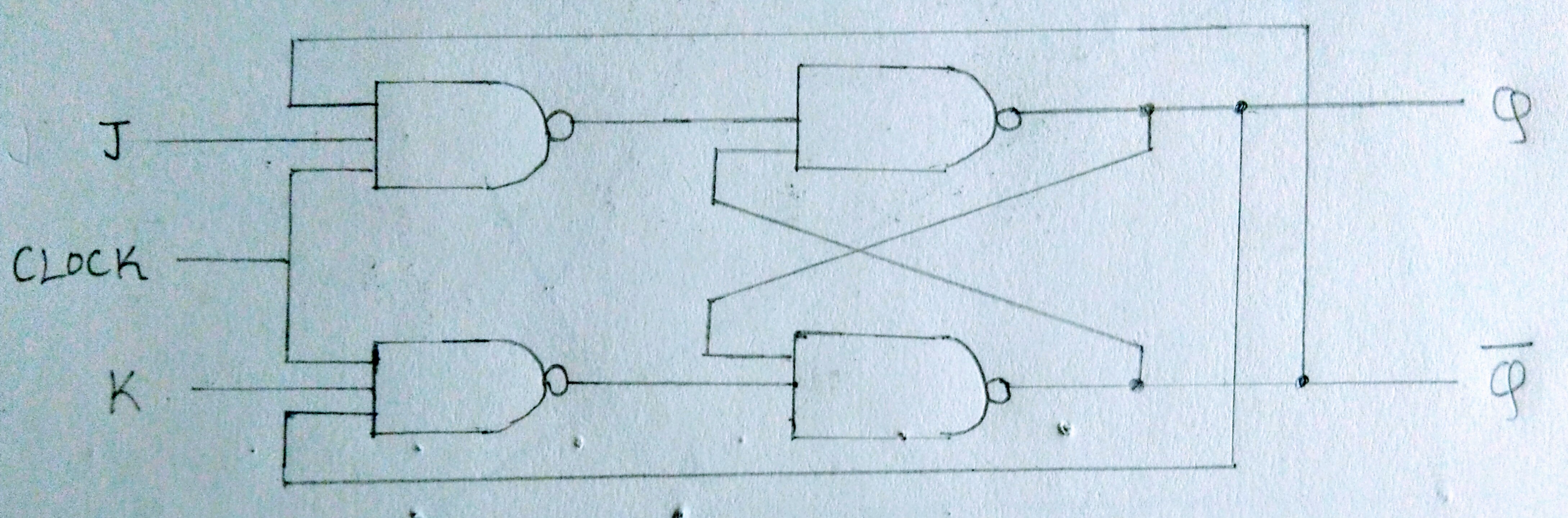
**TFF Truth Table**

|  |  |
| --- | --- |
| **T** | **O/P** |
| 0 | Qn |
| 1 | Qn’ |

|  |  |  |
| --- | --- | --- |
| **T** | **Qn** | **Qn+1** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



**Diagram of JK Flip Flop using NAND gates:**



**Conclusion:**

JK flip flop, D and T flip flops were verified using NAND gates and IC 7376.

**Post Lab Descriptive Questions**

1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?
2. What is use of characteristic and excitation table?
3. How many flip flops due you require storing the data 1101?
4. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

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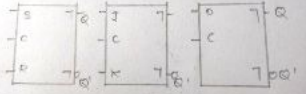
* + - 1. The main difference between a JK flip-flop and an SR flip-flop is that in the JK flip-flop, both inputs can be HIGH. When both the J and K inputs are HIGH, the Q output is toggled, which means that the output alternates between HIGH and LOW. In SR flip-flop is that both inputs shouldn't be HIGH when the clock is triggered. This is considered an invalid input condition, and the resulting output isn't predictable if this condition occurs.
      2. In electronics design, an excitation table shows the minimum inputs that are necessary to generate a particular next state when the current state is known. They are similar to truth tables and state tables, but rearrange the data so that the current state and next state are next to each other on the left-hand side of the table, and the inputs needed to make that state change happen are shown on the right side of the table. A characteristic table has the control input (D or T) as the first column, the current state as the middle column, and the next state as the last column. Basically, it tells you how the control bit affects the current state to produce the next state. An excitation table has the current state as the first column, the next state as the second column, and the control bit as the third column. Basically, think of this as the state you have (first column), the state you want (second column) and what you must set the control bit (third column) to get the desired state you want.
      3. The number of flip flops(n) required for a desired MOD number-N is found out using the equation:

2n-1≤ N ≤2n

where n is the number of flip flops required. We will require 4 JK flip flops to store 1101. This is because 1101 is a 4 bit number and each flip flop can store 1 bit only.

* + - 1. **Edge-triggered flip-flops**: It changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The three basic types are introduced here: S-R, J-K and D. Notice the small triangle, called the dynamic input indicator, is used to identify an edge-triggered flip-flop. Positive edge-triggered (without bubble at Clock input): S-R, J-K, and D. Negative edge-triggered (with bubble at Clock input): S-R, J-K, and D. The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are called asynchronous inputs, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, these asynchronous inputs must both be kept LOW.

**Pulse-Triggered Flip-flops**: The term pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. As this kind of flip-flops are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulse rising edge and must not be changed before the falling edge. Otherwise, ambiguous results will happen. The three basic types of pulse-triggered flip-flops are S-R, J-K and D. Their logic symbols are shown below. Notice that they do not have the dynamic input indicator at the clock input but have postponed output symbols at the outputs.

Edge-triggered flip flop Pulse-triggered flip flop